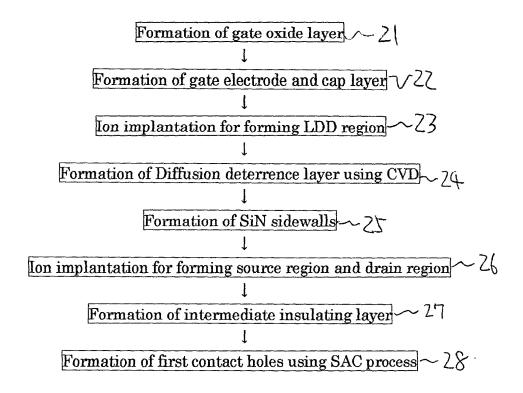


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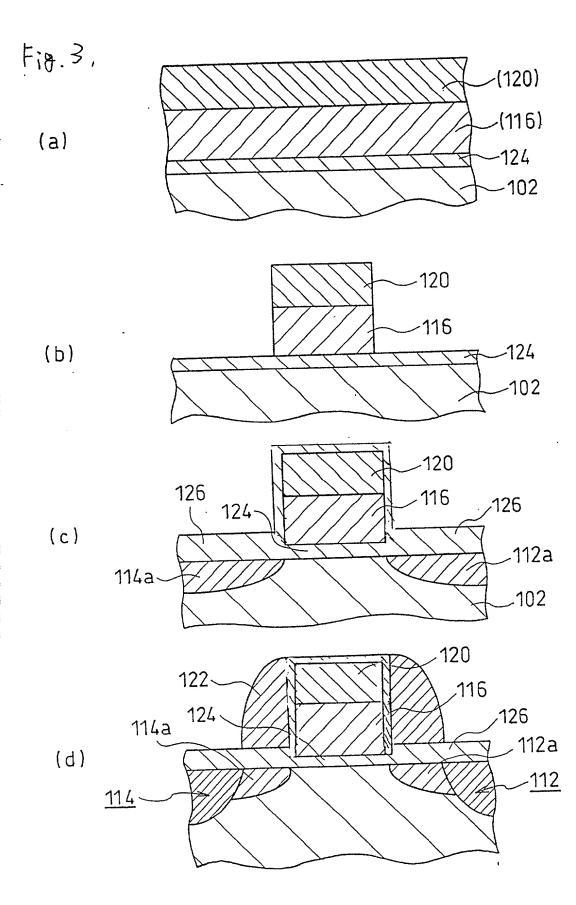
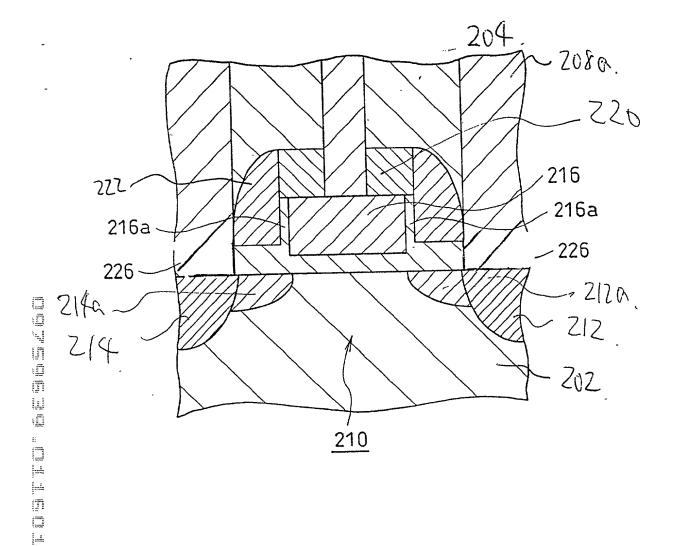
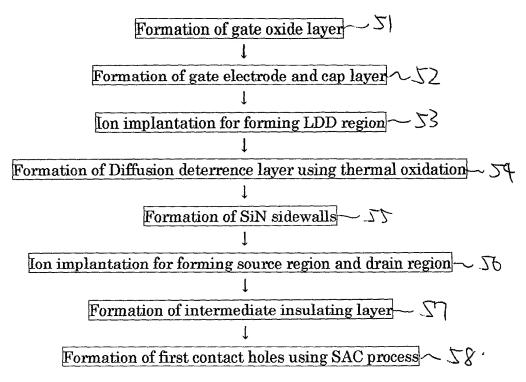
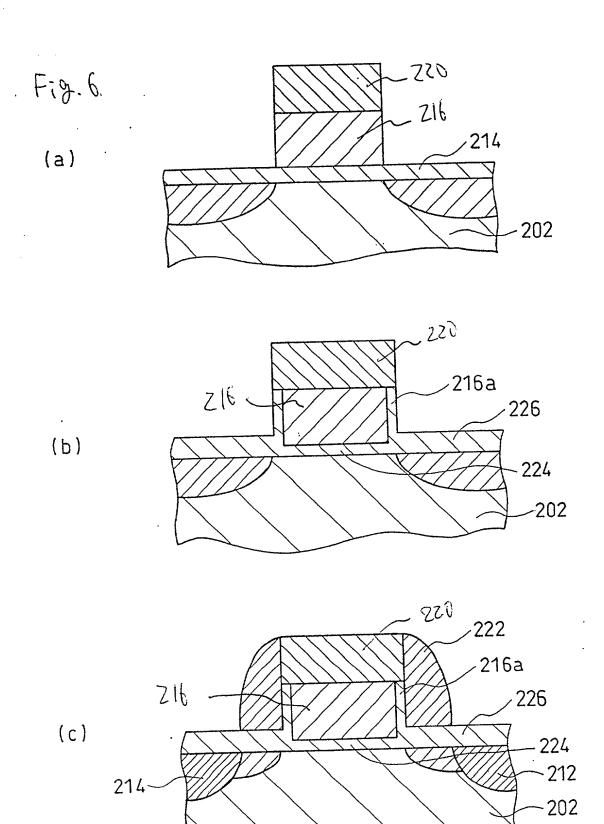


Fig. 4.



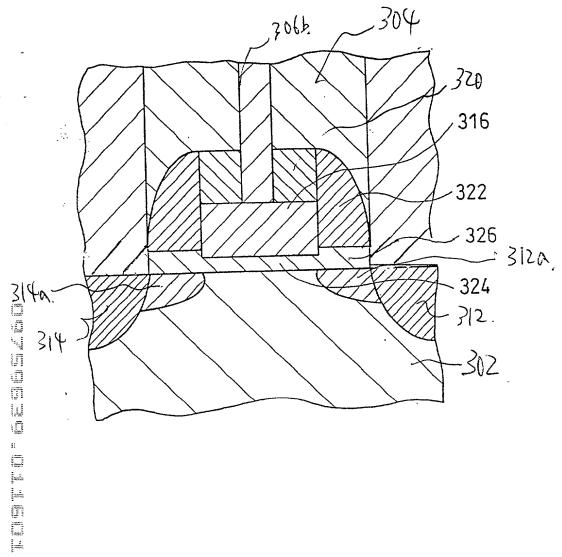
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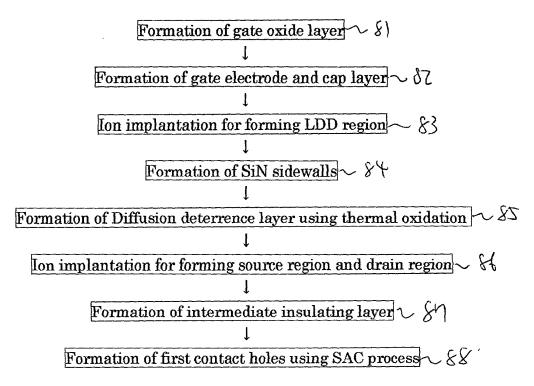


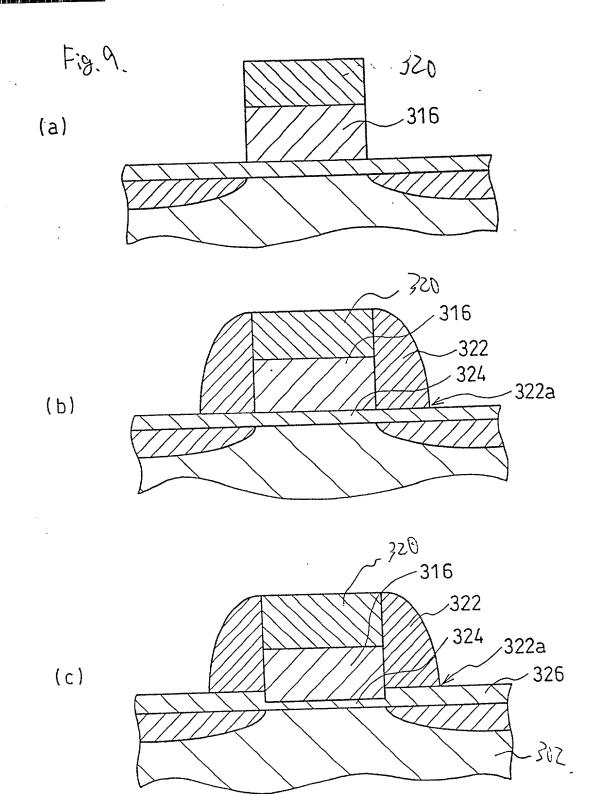


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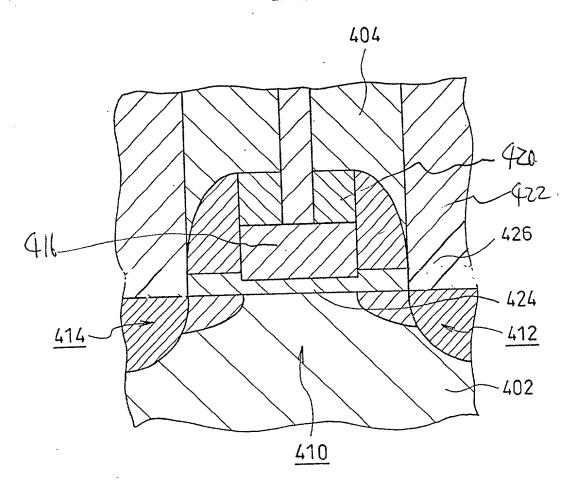
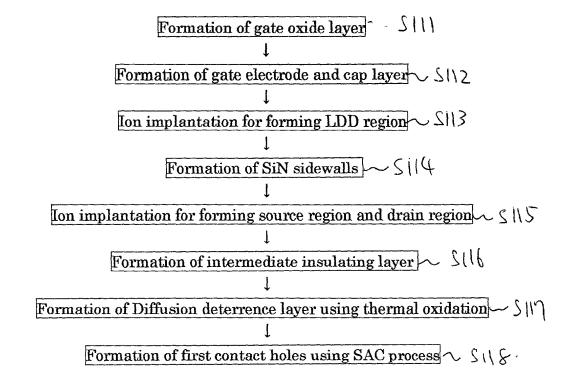
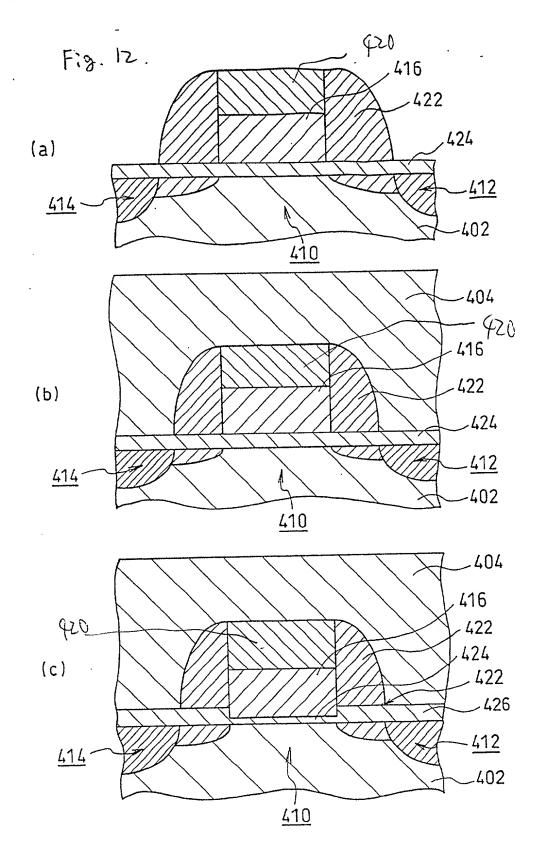


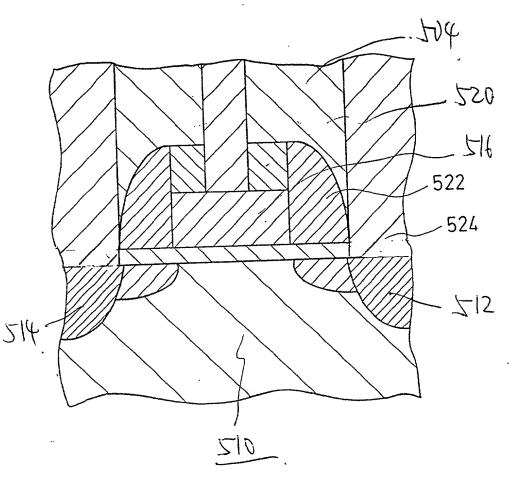
Fig. 11





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Formation of gate oxide layer ~ \$\( \) \\

Formation of gate electrode and cap layer ~ \$\( \) \\

Ion implantation for forming LDD region ~ \$\( \) \\

Formation of SiN sidewalls at over the temperature of 850°C ~ \$\( \) \\

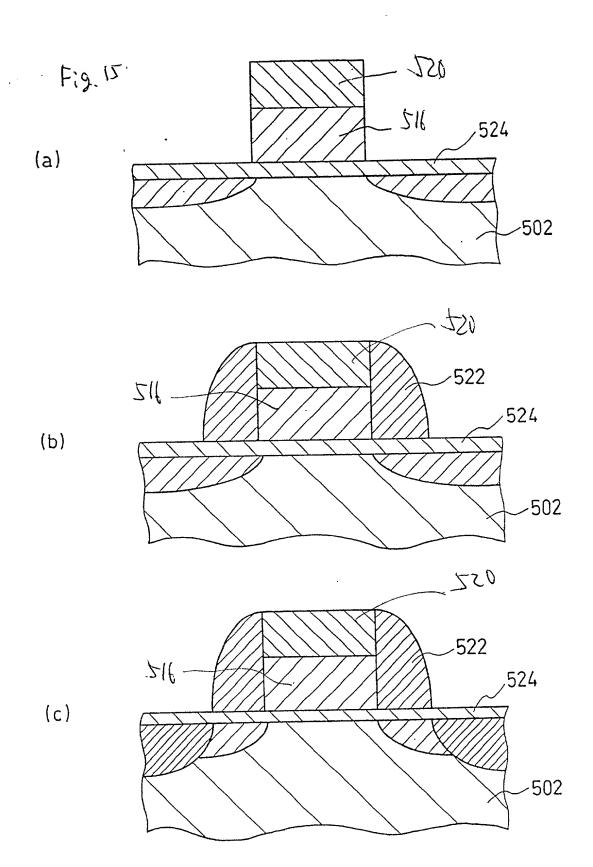
Ion implantation for forming source region and drain region ~ \$\( \) \\

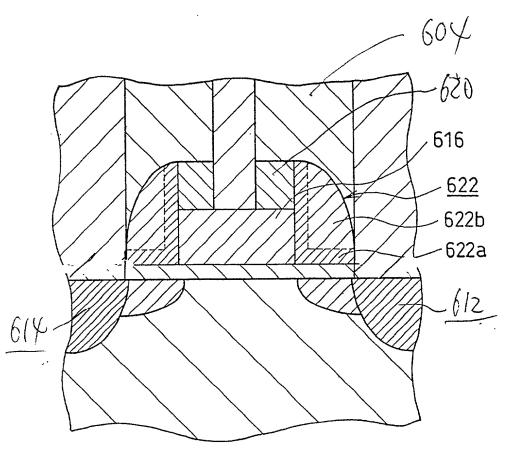
Formation of intermediate insulating layer ~ \$\( \) \\

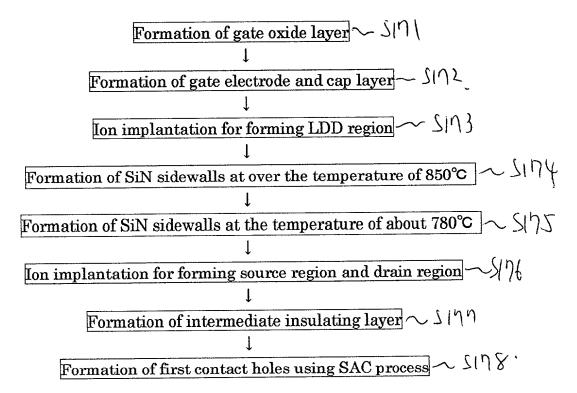
Formation of first contact holes using SAC process ~ \$\( \) \\

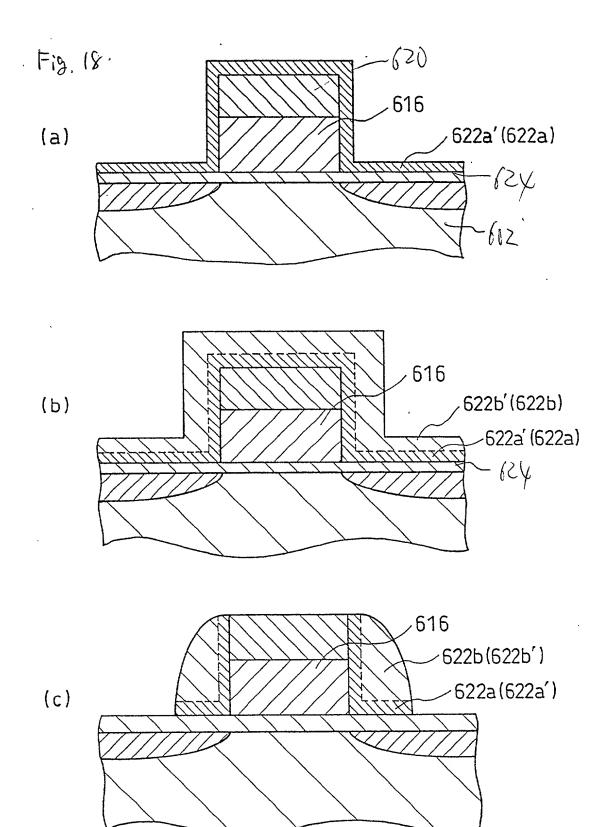
Formation of first contact holes using SAC process ~ \$\( \) \\

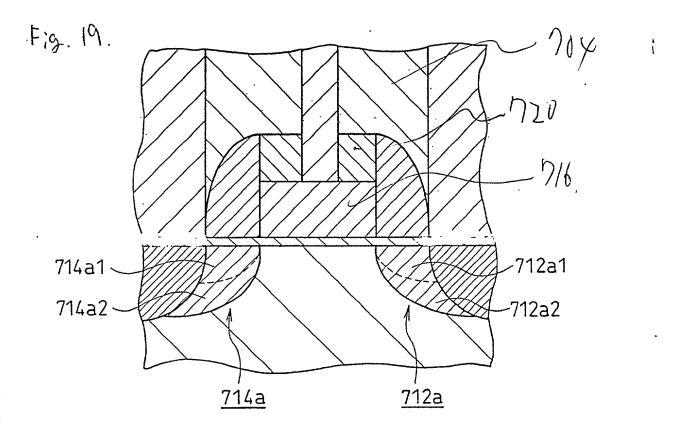
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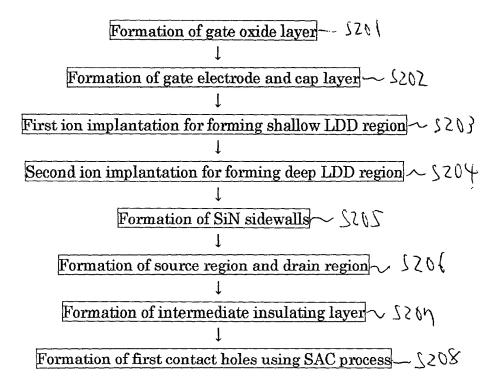


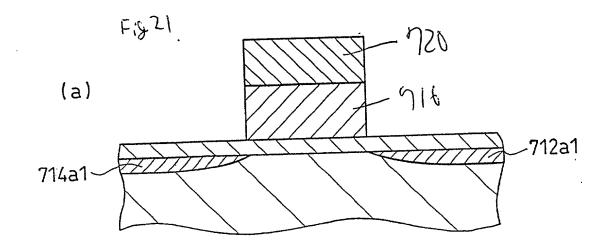


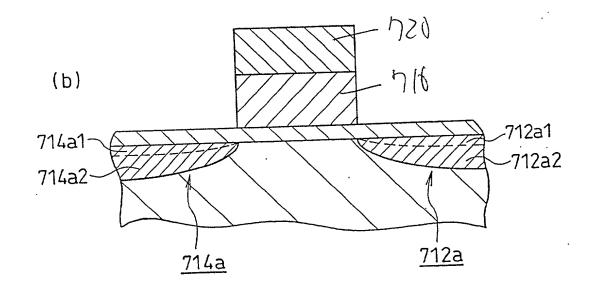


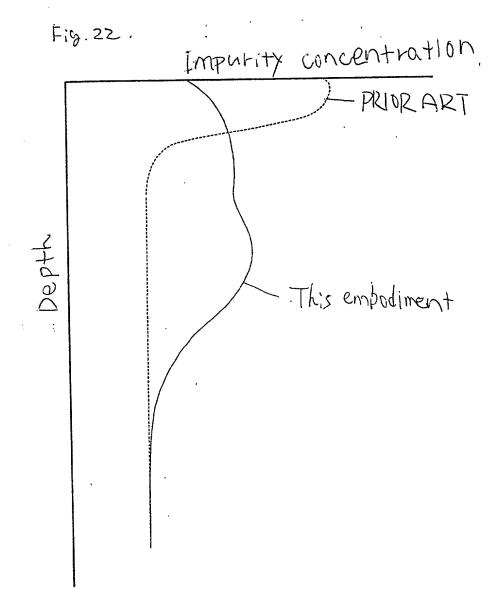




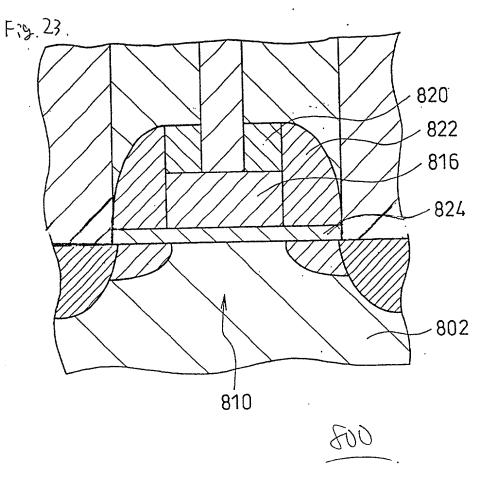








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